

**Birla Vishvakarma Mahavidyalaya**

**Engineering Collage (An Autonomous Institution)**

**Vallabh Vidyanagar - 388 120**

**Affiliated to Gujarat Technological University**

**A.Y. 2023**

# Assignment : I

**Course Title:** Digital System Design

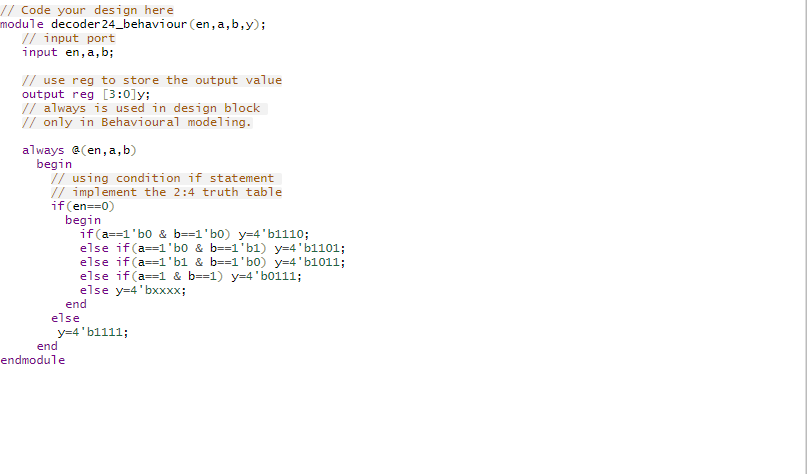
**Name:** Akshay Singh

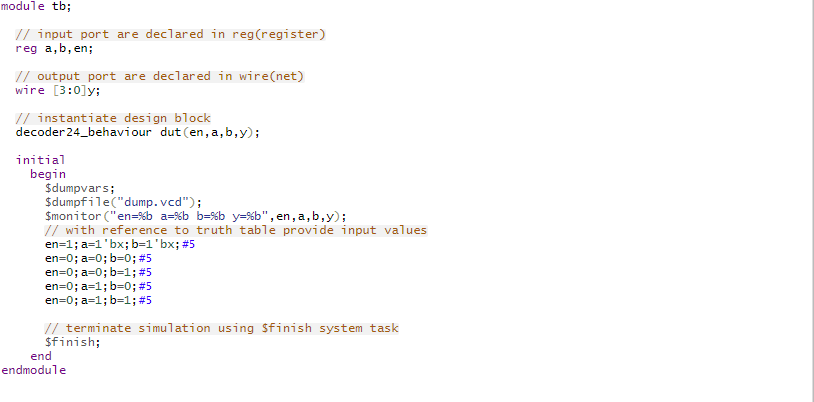
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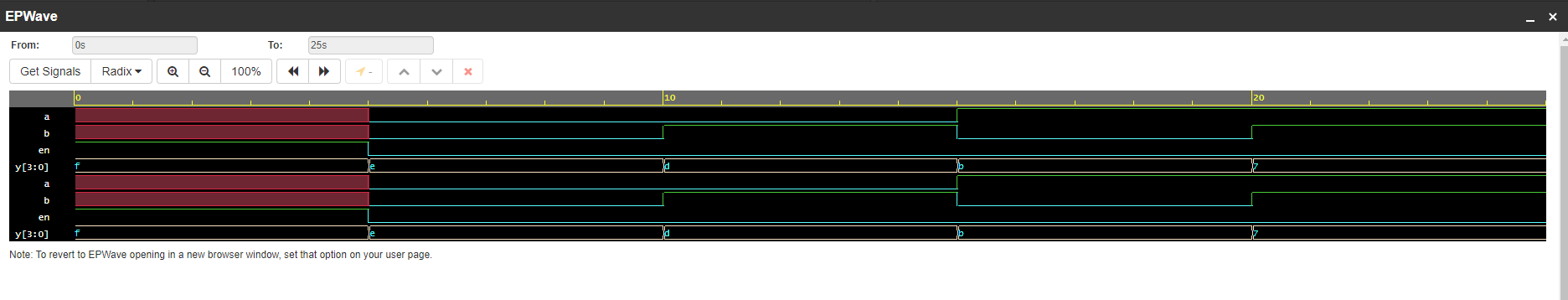
**Batch:** A11

**Course Code:** 3EL42

**Q.1) Write a Verilog code for 2 x 4 Decoder.**

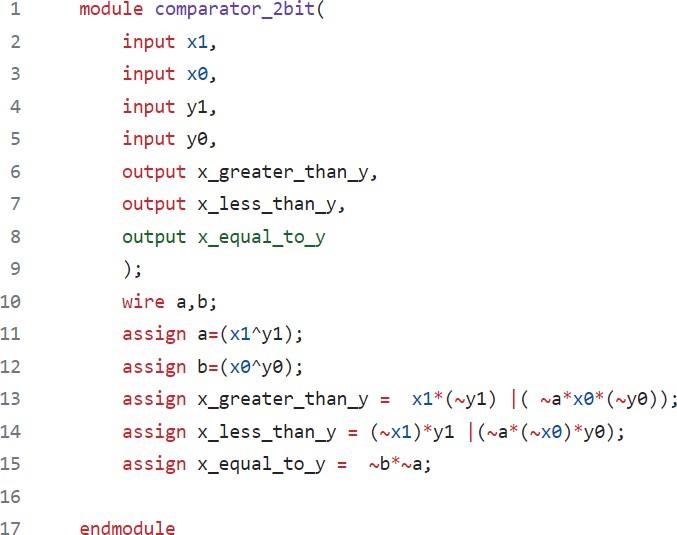




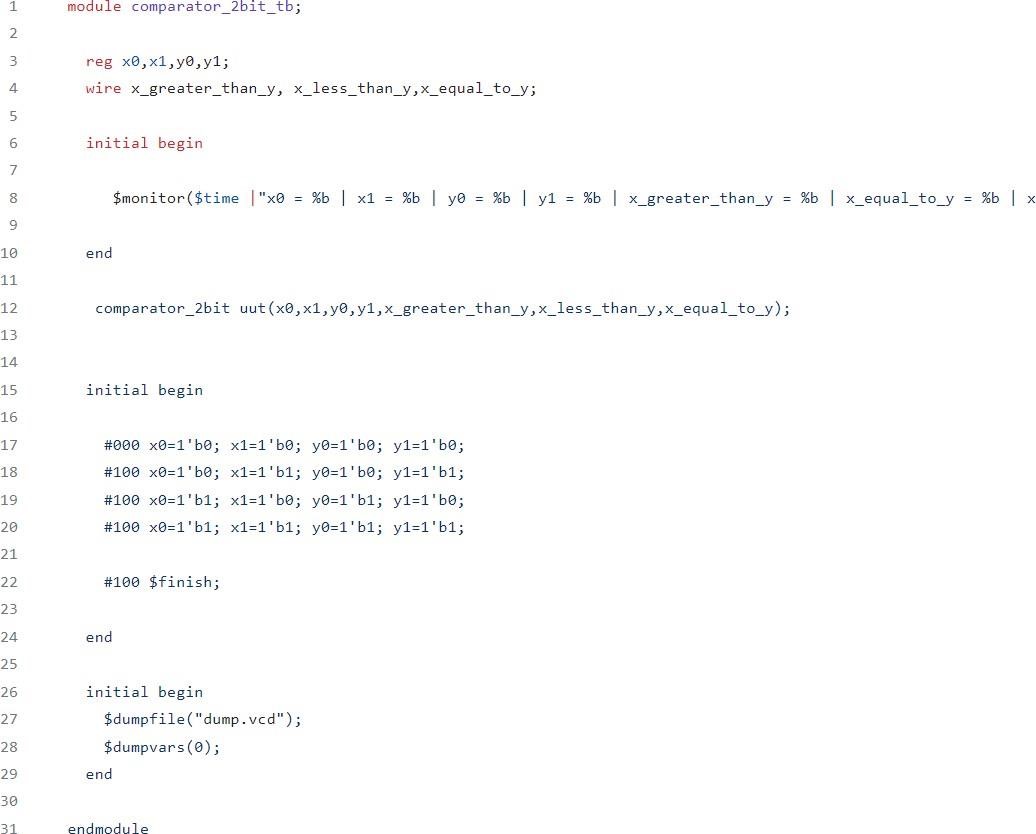


**Q.2) Write a Verilog code for 2-bit comparator.**

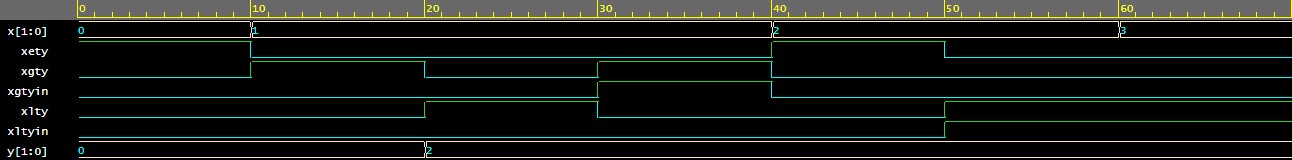
**CODE:**



**TESTBENCH:**

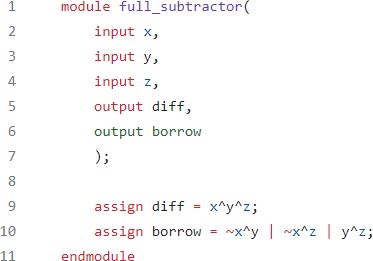


**OUTPUT:**

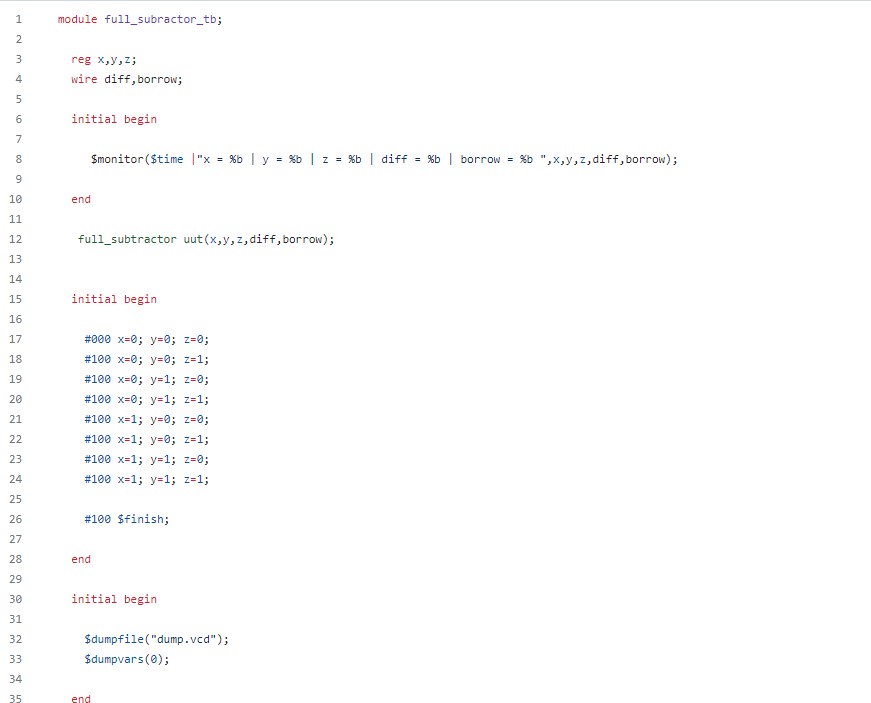


**Q.3) Write a Verlog code for Full Subtractor.**

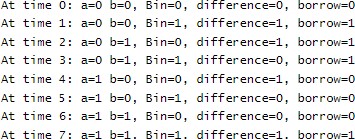
**CODE:**



**TESTBENCH:**

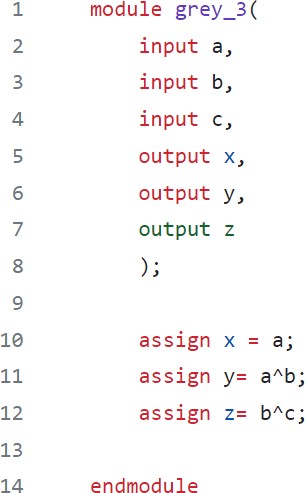


**OUTPUT:**

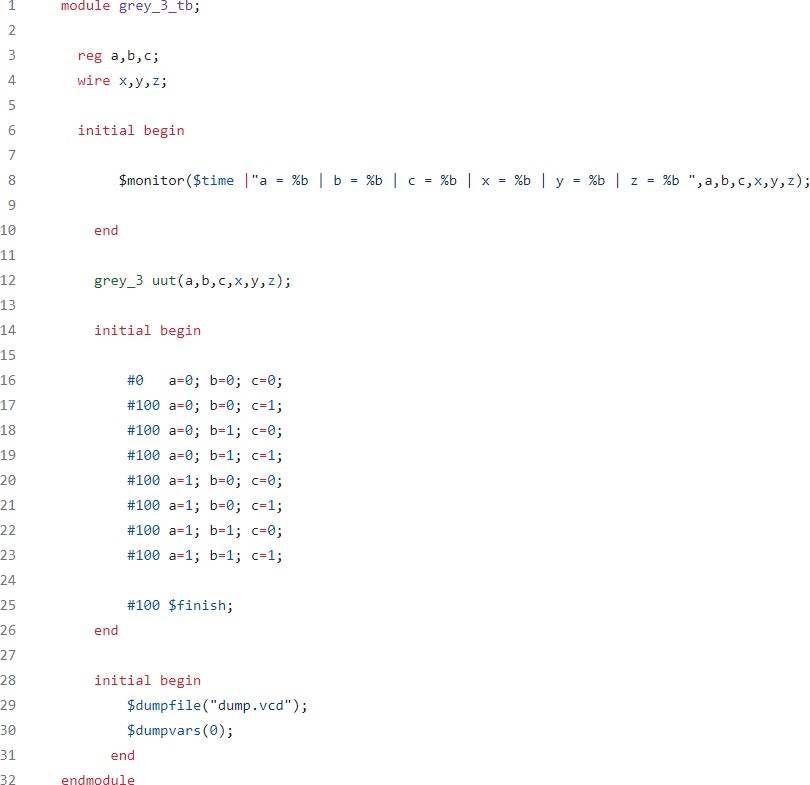


**Q.4) Write a Verilog code for 3 bit binary to gray converter.**

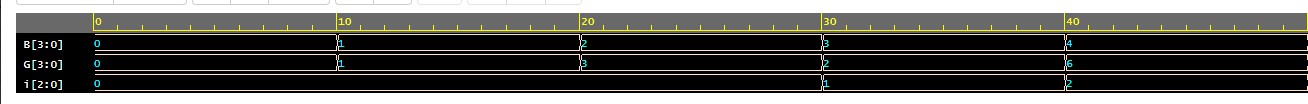
**CODE:**



**TESTBENCH:**

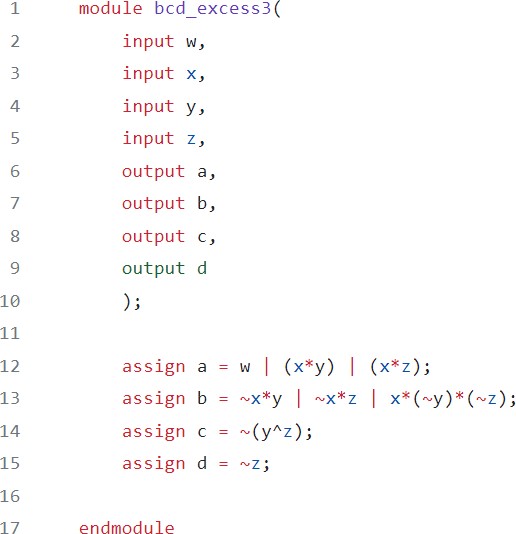


**OUTPUT:**

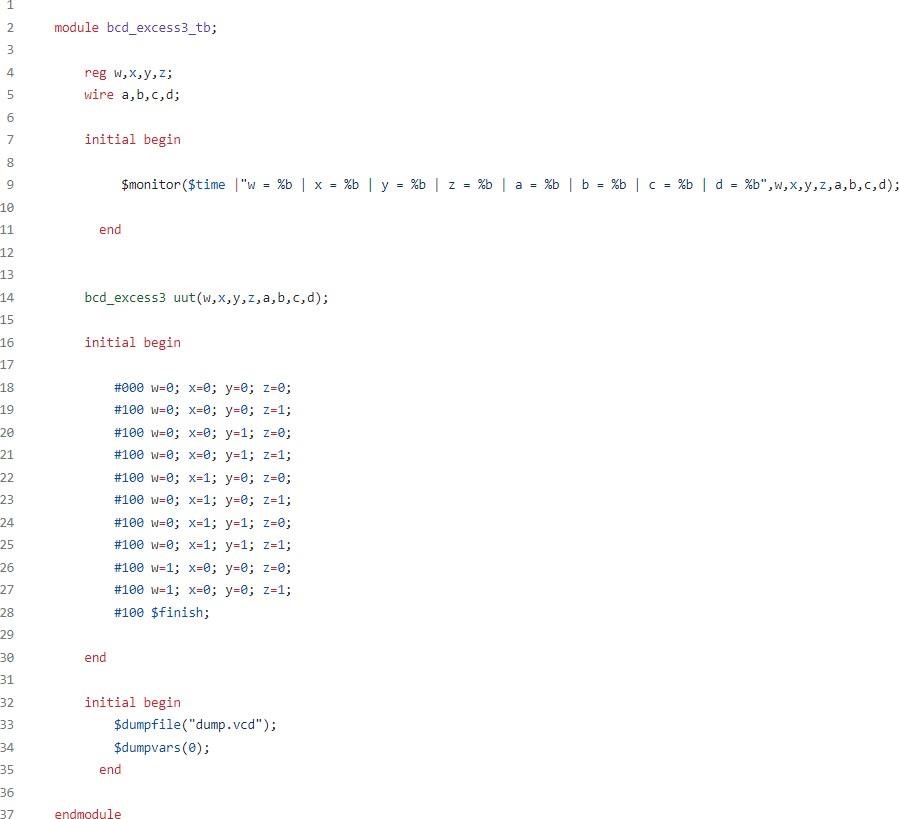


**Q.5) Write a Verilog code for BCD to excess 3 converter.**

**CODE:**



**TESTBENCH:**



**OUTPUT:**

